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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,329	07/02/2002	Ilia Greenblat	56162.000367	8288

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EXAMINER	
NGUYEN, MINH CHAU	
ART UNIT	**PAPER NUMBER**
2145	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,329	GREENBLAT, ILIA	
	Examiner	Art Unit	
	MINH-CHAU N. NGUYEN	2145	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. US 2003/0200342 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

- In the application, it claimed the plurality of ring members including a CPU and at least one peripheral that exchanges date with the CPU. Even though, it doesn't mention about an interface, but the communication between the CPU and peripheral device must have an interface.

- In the copending application, it claimed an external ring interface which enables communication with at least one external peripheral device.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshiyama (5,461,608).

3. Regarding claim 1, Yoshiyama teaches a rings-based system on a chip, comprising:

a plurality of ring members on a ring that communicate using point-to-point connectivity (Col. 1, L. 25-34; and Col. 2, L. 43-65; and figure 1, 5A-C);

a message traversing the ring from member to member (Col. 1, L. 25-60);

the system being adapted so that upon the message arriving at a given ring member the message is processed by that member if the message is applicable to that ring member, and if the message is not applicable to that ring member, the message is passed on to the next ring member (Col. 3, L. 10-49);

the system being adapted to process both read messages and write messages (i.e. in each node, the packet, is received from the source node 11, is extracted to compare with the identifier of the node. If it matches, it will send a response packet to node 11 according to the content of the message. That means each node has to read message before it can send the response packet. Moreover, in

figure 3, step 31, the node 11 sends an alarm collection command message to node 12. That means the node 11 has to write the message which is stored in the memory 26 before it can send the message. Thus, the system is adapted to process both read and write message) (Col. 3, L. 10-Col. 4, L. 12);

the plurality of ring members including a CPU and at least one peripheral that exchanges date with the CPU (i.e. an overhead processor is a CPU; and at least one peripheral is a packet routing and assembly deassembly unit (PRAD) 25) (Col. 2, L. 65-Col. 3, L. 10);

wherein the peripheral includes at least one status memory that stores data describing the status of the peripheral (i.e. the status memory is a ring status memory 26) (Col. 2, L. 65-Col. 4, L. 20);

and wherein the system is configured to write ahead status changes that are accessible by the CPU (i.e. when a fault has occurred, the fault detector notifies it to the PRAD unit 25 (which is connected to the processor) to change the status of the node. It is equivalent to the system write ahead status changes) (Col. 2, L. 65-Col. 4, L. 20).

4. Regarding claim 2, Yoshiyama teaches the system of claim 1, wherein the status memory comprises at least one status register (Inherently, the status memory in a node must have a status register to store the status data) (Col. 3, L. 5-Col. 4, L. 20).

5. Regarding claim 3, Yoshiyama teaches the system of claim 1, wherein the system is adapted to perform write ahead status changes that would otherwise be initiated by the CPU as read operations (i.e. in figure 3, at step 33, the node 11 updates the status data in the ring status memory 26 according to the received alarm message of node 12. Inherently, the CPU in the node 11 must read the received message before it can update (write) the status change in the memory 26) (Col. 3, L. 10-Col. 4, L. 20).

6. Regarding claim 4, Yoshiyama teaches the system of claim 1, wherein the system is adapted to write ahead status changes to a RAM on the CPU or a RAM that is accessible by the CPU (i.e. the system is adapted to update status changes to the ring status memory 26 which is accessible by the CPU. Inherently, updating includes writing; and the ring status memory 26, which allows the data to be stored or accessed, is a RAM) (Col. 3, L. 10 - Col. 4, L. 20).

7. Regarding claim 5, Yoshiyama teaches the system of claim 1, wherein the write ahead operations are performed for some peripheral status changes but not other peripheral status changes (i.e. the write (update) ahead operations are performed for the ring status memory but not for the fault detector. In figure 3, at step 33, the node 11 receives the alarm message of node 12, it updates the status memory 26. However, if the node 11 doesn't receive the alarm message,

the fault detector 27 send the same command message of node 11 to node 15 (at step 36)) (Col. 3, L. 10 - Col. 4, L. 20).

8. Regarding claim 6, Yoshiyama teaches the system of claim 5, wherein the write ahead operation is performed or not performed depending on the nature of the status change (ie. in figure 3, step 32 and 36. The write (update) operation is performed or not performed depending on the alarm message is received by node 12 or not) (Col. 3, L. 10 - Col. 4, L. 20).

9. Regarding claim 7, Yoshiyama teaches the system of claim 5, wherein the write ahead operation is performed or not performed based on the magnitude or the quantity of the status change (i.e. in figure 3, step 32 and 36. The write (update) operation is performed or not performed depending on the alarm message is received by node 12 or not. The alarm message is equivalent to the quantity of the status change. If the alarm message is received, that means the status change is importance, otherwise it is regular) (Col. 3, L. 10 - Col. 4, L. 20).

10. Claim 8 is a corresponding claim of claim 3. Therefore, it is rejected under the same rationale.

11. Regarding claim 11, Yoshiyama teaches a method for processing in a rings based communication system, comprising:

identifying at least one module in a ring network that includes status registers that store status information of regular interest to a processor in the ring network (i.e. the ring status memory 26 is a module in a ring network. Inherently, the status memory in a node must have at least status register to store the status information) (Col. 3, L. 5-Col. 4, L. 20);

identifying which status information can be transmitted to the processor as a write ahead operation initiated by the at least one module instead of a read operation initiated by the processing (i.e. the status information according to the received alarm message of node 12 is transmitted to the processor of node 11 as a write (update) ahead operation performed by the ring status memory 26) (Col. 3, L. 5-Col. 4, L. 20);

programming the at least one module to transmit the identified status information as a write ahead operation (i.e. the status memory of each node 12-15 transmit its status information as the alarm message to the node 11. The node 11 updates the ring status memory 26 as a write ahead operation for the status changes) (Col. 3, L. 5-Col. 4, L. 20).

12. Claims 12 and 13 are corresponding method claim of system claims 6 and 7. Therefore, they are rejected under the same rationale.

13. Regarding claim 14, Yoshiyama teaches the method of claim 11, wherein the step of programming causes the average number of read operations initiated by

the processor to decrease (i.e. Before the node 11 updates the data into the ring status memory 26, it has to read the status information which is sent from other nodes. Inherently, when the node 11 read these data and write it into memory, the number of read operations is decrease) (Col. 3, L. 5-Col. 4, L. 20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 9-10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiyama (5,461,608) as applied to claims 1 and 11 above, and further in view of Boucher et al. (Boucher) (US 6,247,060 B1).

15. Regarding claim 9, Yoshiyama teaches the CPU in a communications chip (ie. The overhead processor 21 is the CPU) (Col. 2, L. 65 – Col. 3, L. 10). Yoshiyama fails to teach the CPU comprises a control protocol processor. However, in the same field of endeavor having closely related objectivity, Boucher teaches the CPU comprises a control protocol processor (Col. 70, L. 4-10).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated Boucher's teachings of the CPU

comprises a control protocol processor, in the teachings of Yoshiyama in the ring network with temporary master node for collecting data from slave nodes during failure, for the purpose of controlling protocol processes, diminishing the ability of the CPU to perform other tasks.

16. Regarding claim 10, Yoshiyama teaches the CPU in a communications chip (Col. 2, L. 65 – Col. 3, L. 10).

Yoshiyama fails to teach the CPU comprises a network processor. However, in the same field of endeavor having closely related objectivity, Boucher teaches the CPU comprises a network processor (Col. 13, L. 25-45).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated Boucher's teachings of comprises a network processor, in the teachings of Yoshiyama in the ring network with temporary master node for collecting data from slave nodes during failure, for the purpose of providing minimizing interrupts and increasing the speed of transmitting messages to a network line.

17. Claim 15 is a corresponding method claim of system claim 9 or 10. Therefore, it is rejected under the same rationale.

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

- 6,005,869 Sakai et al. 12-1999
- 5,802,263 Dittmar et al. 09-1998
- 4,553,233 Debuysscher et al. 11-1985

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MINH-CHAU N. NGUYEN whose telephone number is (571)272-4242. The examiner can normally be reached on Monday-Friday from 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, VALENCIA M. WALLACE can be reached on (571)272-6159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Minh-Chau Nguyen
Art Unit: 2145

M.N

V. Martin-Wallace

VALENCIA MARTIN-WALLACE
SUPERVISORY PATENT EXAMINER